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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,792	03/15/2004	Seung-Jae Baik	5649-1240	9199

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,792	BAIK, SEUNG-JAE	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group I (Claims 1-18) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 19-36 are canceled.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the

reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claims 1-7, 9 and 11-12 are rejected under 35 U. S. C. § 102 (e) as being anticipated by Song et al.

Regarding to claims 1-9 and 11-12, Song discloses a memory device comprising a semiconductor substrate (fig. 1(a); a first gate insulator (SiO_2) on a first portion of a semiconductor substrate; a storage node (memory node) on the first gate insulator; a tunnel junction barrier 4 on the storage node; a data electrode (data line) on the tunnel junction barrier 4; a second gate insulator layer on a sidewall of the tunnel junction barrier; a third gate insulator on a second portion of the substrate adjacent the tunnel junction barrier; a gate electrode 11 on the second gate insulator and the third gate insulator; and first and second impurity-doped regions 7, 8 in the substrate coupled by a channel through the first and second portions of the substrate (fig. 1 A and 1D).

Regarding to claim 2, a memory device according to claim 1, wherein the storage node is on a first channel in the first portion of the substrate, and wherein the gate electrode is on a second channel in the second portion of the substrate that couples the first channel to the first impurity-doped region (figs. 1 and 2).

Regarding to claim 3, a memory device according to claim 2, wherein the second channel is configured to serve as a source/drain for the first channel (figs. 1 and 2).

Regarding to claim 4, a memory device according to claim 1, further comprising a fourth gate insulator on a second sidewall of the tunnel junction barrier and a fifth gate insulator on a third portion of the substrate between the tunnel junction barrier and the second impurity-doped region, and wherein the gate electrode is disposed on the fourth and fifth gate insulators (figs. 1 and 2).

Regarding to claim 5, a memory device according to claim 4, wherein the gate electrode is on a third channel region in the third portion of the substrate that couples the first channel to the second impurity-doped region (figs. 1 and 2).

Regarding to claim 6, a memory device according to claim 5, wherein the third channel is configured to serve as a source/drain for the first channel (figs. 1 and 2).

Regarding to claim 7, a memory device according to claim 4, wherein the second, third, fourth and fifth gate insulators comprise respective portions of a continuous insulation layer conforming to a top of the data electrode and to the sidewalls of the tunnel junction barrier and to surfaces of the substrate adjacent thereto, and wherein the

gate electrode comprises a continuous conductive layer overlying the continuous insulation layer (figs. 1 and 2).

Regarding to claim 9, a memory device according to claim 1, wherein the second and third gate insulators comprise respective portions of a continuous insulation layer conforming to the sidewall of the tunnel junction barrier and to a surface of the second portion of the substrate, and wherein the gate electrode comprises a continuous conductive layer overlying the continuous insulation layer (figs. 1 and 2).

Regarding to claim 11, a memory device according to claim 10, further comprising an insulation layer on the data electrode, and wherein the gate electrode comprises a portion on the insulation layer on the data electrode (figs. 1 and 2).

Regarding to claim 12, a memory device according to claim 10, wherein the gate electrode comprises a continuous conductive layer overlying the second and third gate insulators and the data electrode (figs. 1 and 2).

Regarding to claim 13, Song discloses a memory device, comprising a semiconductor substrate; a tunnel junction barrier transistor having a storage node on the substrate, a tunnel junction barrier 4 on the storage node, and a gate electrode on a

sidewall of the tunnel junction barrier that controls a channel of the tunnel junction barrier transistor; a first planar transistor having a first channel in the substrate disposed transverse to the channel of the tunnel junction barrier transistor and controlled by the storage node of the tunnel junction barrier transistor; and a second planar transistor having a second channel in the substrate disposed adjacent to the first planar transistor and transverse to the channel of the tunnel junction barrier transistor and having a gate electrode electrically coupled to the gate electrode of the tunnel junction barrier transistor (figs 1 and 2).

Regarding to claim 14, a memory device according to claim 13, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a continuous conductive layer having a first portion on the sidewall of the tunnel junction barrier and a second portion that extends transverse to the first portion onto the channel of the second planar transistor (figs. 1 and 2).

Regarding to claim 15, a memory device according to claim 13, wherein the second planar transistor comprises second channels on respective sides of the first channel (figs. 1 and 2).

Regarding to claim 16, a memory device according to claim 15, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor

comprise a first continuous conductive layer having a first portion on a first sidewall of the tunnel junction barrier and a second portion that extends transverse to the first portion onto a first one of the second channels of the second planar transistor, and a second continuous conductive layer having a first portion on a second sidewall of the tunnel junction barrier opposite the first sidewall and a second portion that extends transverse to the first portion onto a second one of the second channels of the second planar transistor (figs. 1 and 2).

Regarding to claim 17, a memory device according to claim 15, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a continuous conductive layer disposed on first and second opposing sidewalls of the tunnel junction barrier and on respective portions of the substrate adjacent the first and second sidewalls (figs. 1 and 2).

Regarding to claim 18, a memory device according to claim 15, further comprising respective first and second impurity doped regions in the substrate on respective sides of the tunnel junction barrier transistor and electrically coupled to respective ones of the second channels (figs. 1 and 2).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,528,896 to Song et al. in view of Kim et al. (6,475,857).

Regarding to claims 8 and 10, Song discloses the claimed invention except for the memory device, wherein the gate electrode further comprises conductive sidewall spacers interposed between the portions of the second insulation layer on the sidewalls of the tunnel junction barrier and the continuous conductive layer.

Kim discloses the memory device, wherein the gate electrode further comprises conductive sidewall spacers interposed between the portions of the second insulation layer on the sidewalls of the tunnel junction barrier and the continuous conductive layer (col. 11, lines 30-40, and fig. 5(b)).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory device, wherein the gate electrode further comprises conductive sidewall spacers interposed between the portions of the second insulation layer on the sidewalls of the tunnel junction barrier and the continuous conductive layer, as taught by Kim in order to form a semiconductor memory device

having memory cells that allow scalable memory charge relative to cell density of the device with long-term retention, low voltage, high speed, and highly reliable operational characteristics (col. 1, lines 37-42).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran